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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,984	09/25/2006	Ralf Lerner	P28504	2111

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
05/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/552,984	LERNER, RALF	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

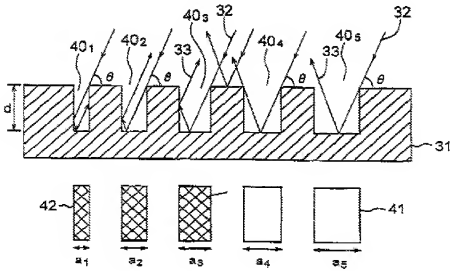
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kishimura U.S. Patent Application Publication 2002/0097405 A1.

Kishimura discloses a semiconductor device and semiconductor process as claimed. Please see FIGS. 1-8B, where Kishimura teaches the following limitations.



Pertaining to claim 1, Kishimura teaches a test structure for verifying an isolation trench etching

in an SOI wafer, wherein the test structure comprises, after etching of isolation trenches, a row of connected islands, each of which is surrounded by a trench, said trenches having an (step-wise) increasing width from island to island (A, B; B,C), including a trench width of an isolation trench of an active circuit;

- wherein a section (part) of the surrounding trench (a, b) of each island (A, B) forms a common part with the trench of the adjacent island;
- wherein the respective section - except for the island having the broadest (e) or the narrowest (a) isolation trench - has the width of the adjacent trench having the next larger or the next smaller measure of width in the row (please note that the semiconductor wafer of Kishimura inherently includes silicon-on-insulator, since the term is well known during the invention of Kishimura).

Pertaining to claim 2, Kishimura teaches a method of verifying insulation trench etchings or isolation trench etchings in SOI substrates, comprising

- forming a test structure comprising a row of successive islands during an etch process or preparing the test structure for an etch process and measuring an electric pass several times during or after said trench etching;
- wherein a plurality of measurements of the electric pass are performed;
- wherein one of the measurements is performed between two adjacent islands (A, B), a further measurement is performed between other adjacent islands (B, C);

using measurement values of said plurality of measurements for assessing a sufficient or

appropriate depth of etched insulation trenches or isolation trenches located in particular outside said test structure above said substrate in an area of an active circuit.

Pertaining to claim 3, Kishimura teaches a method for verifying trench etchings (isolation trench, insulation trench) in an SOI substrate, comprising

- preparing a test structure (A, B, D, E) above the substrate and forming the test structure during a trench etching and measuring after or during said trench etching an electric pass particularly successively between an island (A, B) and the substrate region (S) at least partially surrounding said island and
- using the magnitude or the amount of the measurement results for assessing or detecting a sufficient or appropriate depth of etched trenches located in particular outside said test structure but being formed during said trench etching.

Pertaining to claim 4, Kishimura teaches the method of claim 2, wherein said test structure comprises, after etching of isolation trenches, a row of connected islands, each of which is surrounded by a trench, said trenches having an (step-wise) increasing width from island to island (A, B; B,C), including a trench width of an isolation trench of an active circuit;

- wherein a section (part) of the surrounding trench (a, b) of each island (A, B) forms a common part with the trench of the adjacent island;
- wherein the respective section - except for the island having the broadest (e) or the narrowest (a) isolation trench - has the width of the adjacent trench having the next larger or the next smaller measure of width in the row.

Pertaining to claim 5, Kishimura teaches the method of claim 2, wherein said electric pass is a resistance or a conductance.
Pertaining to claim 6, Kishimura teaches the method of claims claim 2, wherein said pass is a current at a constant voltage or a voltage measurement at a constant current.

Pertaining to claim 7, Kishimura teaches the method of claim 2, wherein the measurements are performed during the etch process, and wherein the etch process is interrupted to perform in particular the successive measurement on the islands.

Pertaining to claim 8, Kishimura teaches the method of claim 7, wherein the etching (etch process) is continued when the trench having a width (d) corresponding to the present circuit is not completely etched through to the insulating layer.

Pertaining to claim 9, Kishimura teaches the method of claim 7, wherein the etching is stopped, when the trench having a width (d) corresponding to the active circuit is etched through to the insulating layer.

Pertaining to claim 10, Kishimura teaches a method for verifying insulation trench etchings in SOI wafers, in which dedicated devices or complete circuit modules are laterally dielectrically isolated in the form of islands from the surrounding region by enclosing insulation trenches (8); by a test structure prepared on an individual wafer, for performing a verification of the electric

resistances or resistance during a process step "insulation trench etch process"
between specific regions (A,B; B,C) of the test structure and/or between specific regions of the test structure and the surrounding crystal region (S)
the method further comprising
preparing the test structure on the wafer, said test structure having a row of connected islands after the trench etch process of the process step "insulation trench etch process", each island being surrounded by a trench having a different width between respective two of said islands; wherein the width of the insulation trench provided in the active circuit is positioned approximately in a central location within said row of islands,
and a portion of the length of the surrounding trench of each island, except for the outer most island, defines a shared piece of the island of a respective adjacent island such that said portion of the length particularly corresponds to the width of the adjacent trench having the next larger or the next smaller measure of width in the row;
- after the etch process of the "insulation trench etch process", assessing a proper process result by repeatedly verifying the electric pass between respective two adjacent islands or between a respective island and the surrounding (S) of said respective island outside of said test structure;
- using an amount of one or more detected measurement values of the measurement as a measure or a test for the target depth, in particular for the predefined depth, of etched insulation trenches or isolation trenches.

Pertaining to claim 11, Kishimura teaches the method of claim 10, wherein the width of each

trench surrounding a respective island in the row of islands receives an increasing width that increases in a step-wise manner from island to island.

Pertaining to claim 12, Kishimura teaches the method of claim 10, wherein a width of the insulation trench occurring in the active circuit is predefined as a "relevant width of insulation trenches".

Pertaining to claim 13, Kishimura teaches the method of claim 2, wherein, during a successive measurement of passes, it is started with an island having a surrounding trench width (d) that substantially corresponds to one or more relevant insulation trenches of the circuit.

Pertaining to claim 14, Kishimura teaches the method of claims claim 2, wherein the step of verifying is completed after two measurements, when an abrupt change of the pass value for the total insulation (etching through the insulating layer) is obtained for the relevant pair of islands of the test structure, and when testing the adjacent pair of islands having the smaller trench width does not exhibit said abruptly changed measurement value.

Pertaining to claim 15, Kishimura teaches the method or the test device of any claims claim 2, wherein at least three, preferably five or more island regions (A to E) are connected to each other.

Pertaining to claim 16, Kishimura teaches the method of claim 2, wherein not more than n-1 measurements are performed for the n islands, n being the number of islands in said row.

Pertaining to claim 17, Kishimura teaches the method of claim 2, wherein the maximum number of measurements between islands and the surrounding (S) corresponds to the number of islands in the row of islands.

Pertaining to claim 18, Kishimura teaches the method of claim 2, wherein after the etch process the measurement results are evaluated, and wherein particularly further etch processes of following wafers are adapted with respect to their target etch time to the result of the preceding measurements.

Pertaining to claim 19, Kishimura teaches the method of claim 10, wherein the step of preparing is performed by a predetermined mask.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishimura U.S. Patent Application Publication 2002/0087405 A1 in view of Wise et al., U.S. Patent 6,821,865 B2.

Kishimura discloses a semiconductor device and semiconductor process substantially as claimed as discussed above. However, Kishimura uses the term semiconductor wafer which will include silicon-on-insulator. Wise is included to further disclose how well known silicon-on-insulator (SOI) can be interchanged with the term semiconductor wafer.

Pertaining to claim 1, Kishimura teaches a test structure for verifying an isolation trench etching in an SOI wafer, wherein the test structure comprises, after etching of isolation trenches, a row of connected islands, each of which is surrounded by a trench, said trenches having an (step-wise) increasing width from island to island (A, B; B,C), including a trench width of an isolation trench of an active circuit;

- wherein a section (part) of the surrounding trench (a, b) of each island (A, B) forms a common part with the trench of the adjacent island;
- wherein the respective section - except for the island having the broadest (e) or the narrowest (a) isolation trench - has the width of the adjacent trench having the next larger or the next smaller measure of width in the row (please note that the semiconductor wafer of Kishimura inherently includes silicon-on-insulator, since the term is well known). Wise teaches the term silicon-on-insulator (SOI). In view of Wise it would have been obvious to one of ordinary skill in the art to randomly select and SOI wafer for a semiconductor wafer because SOI substrates are included in the category of semiconductor wafers (see column 2, lines 53-55 of Wise).

Pertaining to claim 2, Kishimura teaches a method of verifying insulation trench etchings or isolation trench etchings in SOI substrates, comprising

- forming a test structure comprising a row of successive islands during an etch process or preparing the test structure for an etch process and measuring an electric pass several times during or after said trench etching;
- wherein a plurality of measurements of the electric pass are performed;
- wherein one of the measurements is performed between two adjacent islands (A, B), a further measurement is performed between other adjacent islands (B, C);

using measurement values of said plurality of measurements for assessing a sufficient or appropriate depth of etched insulation trenches or isolation trenches located in particular outside said test structure above said substrate in an area of an active circuit. (please note that the semiconductor wafer of Kishimura inherently includes silicon-on-insulator, since the term is well known). Wise teaches the term silicon-on-insulator (SOI). In view of Wise it would have been obvious to one of ordinary skill in the art to randomly select and SOI wafer for a semiconductor wafer because SOI substrates are included in the category of semiconductor wafers (see column 2, lines 53-55 of Wise).

Pertaining to claim 3, Kishimura teaches a method for verifying trench etchings (isolation trench, insulation trench) in an SOI substrate, comprising

- preparing a test structure (A, B, D, E) above the substrate and forming the test structure during a trench etching and measuring after or during said trench etching an electric pass particularly

successively between an island (A, B) and the substrate region (S) at least partially surrounding said island and

- using the magnitude or the amount of the measurement results for assessing or detecting a sufficient or appropriate depth of etched trenches located in particular outside said test structure but being formed during said trench etching. (please note that the semiconductor wafer of Kishimura inherently includes silicon-on-insulator, since the term is well known). Wise teaches the term silicon-on-insulator (SOI). In view of Wise it would have been obvious to one of ordinary skill in the art to randomly select and SOI wafer for a semiconductor wafer because SOI substrates are included in the category of semiconductor wafers (see column 2, lines 53-55 of Wise).

Pertaining to claim 4, Kishimura in view of Wise teaches the method of claim 2, wherein said test structure comprises, after etching of isolation trenches, a row of connected islands, each of which is surrounded by a trench, said trenches having an (step-wise) increasing width from island to island (A, B; B,C), including a trench width of an isolation trench of an active circuit;

- wherein a section (part) of the surrounding trench (a, b) of each island (A, B) forms a common part with the trench of the adjacent island;

- wherein the respective section - except for the island having the broadest (e) or the narrowest (a) isolation trench - has the width of the adjacent trench having the next larger or the next smaller measure of width in the row.

Pertaining to claim 5, Kishimura in view of Wise teaches the method of claim 2, wherein said electric pass is a resistance or a conductance.

Pertaining to claim 6, Kishimura in view of Wise teaches the method of claims claim 2, wherein said pass is a current at a constant voltage or a voltage measurement at a constant current.

Pertaining to claim 7, Kishimura in view of Wise teaches the method of claim 2, wherein the measurements are performed during the etch process, and wherein the etch process is interrupted to perform in particular the successive measurement on the islands.

Pertaining to claim 8, Kishimura in view of Wise teaches the method of claim 7, wherein the etching (etch process) is continued when the trench having a width (d) corresponding to the present circuit is not completely etched through to the insulating layer.

Pertaining to claim 9, Kishimura in view of wise teaches the method of claim 7, wherein the etching is stopped, when the trench having a width (d) corresponding to the active circuit is etched through to the insulating layer.

Pertaining to claim 10, Kishimura teaches a method for verifying insulation trench etchings in SOI wafers, in which dedicated devices or complete circuit modules are laterally dielectrically isolated in the form of islands from the surrounding region by enclosing insulation trenches (8); by a test structure prepared on an individual wafer, for performing a verification of the electric resistances or resistance during a process step "insulation trench etch process" between specific regions (A,B; B,C) of the test structure and/or between specific regions of the test structure and the surrounding crystal region (S)

the method further comprising

preparing the test structure on the wafer, said test structure having a row of connected islands after the trench etch process of the process step "insulation trench etch process", each island being surrounded by a trench having a different width between respective two of said islands; wherein the width of the insulation trench provided in the active circuit is positioned approximately in a central location within said row of islands,

and a portion of the length of the surrounding trench of each island, except for the outer most island, defines a shared piece of the island of a respective adjacent island such that said portion of the length particularly corresponds to the width of the adjacent trench having the next larger or the next smaller measure of width in the row;

- after the etch process of the "insulation trench etch process", assessing a proper process result by repeatedly verifying the electric pass between respective two adjacent islands or between a respective island and the surrounding (S) of said respective island outside of said test structure;

- using an amount of one or more detected measurement values of the measurement as a measure or a test for the target depth, in particular for the predefined depth, of etched insulation trenches or isolation trenches. (please note that the semiconductor wafer of Kishimura inherently includes silicon-on-insulator, since the term is well known). Wise teaches the term silicon-on-insulator (SOI). In view of Wise it would have been obvious to one of ordinary skill in the art to randomly select and SOI wafer for a semiconductor wafer because SOI substrates are included in the category of semiconductor wafers (see column 2, lines 53-55 of Wise).

Pertaining to claim 11, Kishimura in view of Wise teaches the method of claim 10, wherein the width of each trench surrounding a respective island in the row of islands receives an increasing width that increases in a step-wise manner from island to island.

Pertaining to claim 12, Kishimura in view of Wise teaches the method of claim 10, wherein a width of the insulation trench occurring in the active circuit is predefined as a "relevant width of insulation trenches".

Pertaining to claim 13, Kishimura in view of Wise teaches the method of claim 2, wherein, during a successive measurement of passes, it is started with an island having a surrounding trench width (d) that substantially corresponds to one or more relevant insulation trenches of the circuit.

Pertaining to claim 14, Kishimura in view of Wise teaches the method of claims claim 2, wherein the step of verifying is completed after two measurements, when an abrupt change of the pass value for the total insulation (etching through the insulating layer) is obtained for the relevant pair of islands of the test structure, and when testing the adjacent pair of islands having the smaller trench width does not exhibit said abruptly changed measurement value.

Pertaining to claim 15, Kishimura in view of Wise teaches the method or the test device of any

claims claim 2, wherein at least three, preferably five or more island regions (A to E) are connected to each other.

Pertaining to claim 16, Kishimura in view of Wise teaches the method of claim 2, wherein not more than n-1 measurements are performed for the n islands, n being the number of islands in said row.

Pertaining to claim 17, Kishimura in view of Wise teaches the method of claim 2, wherein the maximum number of measurements between islands and the surrounding (S) corresponds to the number of islands in the row of islands.

Pertaining to claim 18, Kishimura in view of Wise teaches the method of claim 2, wherein after the etch process the measurement results are evaluated, and wherein particularly further etch processes of following wafers are adapted with respect to their target etch time to the result of the preceding measurements.

Pertaining to claim 19, Kishimura in view of Wise teaches the method of claim 10, wherein the step of preparing is performed by a predetermined mask.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

W. David Coleman
Primary Examiner
Art Unit 2823

/W. David Coleman/
Primary Examiner, Art Unit 2823